What is Claimed is:

1. A programmable logic resource having programmable logic resource core circuitry that provides a reset signal to an intellectual property block that supports a multi-channel input/output protocol comprising:

circuitry for routing the reset signal throughout a plurality of channels in the intellectual property block during a same clock cycle, wherein the reset signal is glitch-free and the circuitry is operative to be skew-tolerant.

2. The programmable logic resource of claim 1 wherein the circuitry comprises combinatorial logic that receives as input the reset signal and outputs a plurality of reset signals, wherein each of the plurality of reset signals is associated with one of the plurality of channels.

3. The programmable logic resource of claim 2 wherein each of the plurality of reset signals comprises a receiver reset signal.

4. The programmable logic resource of claim 2 wherein each of the plurality of reset signals comprises a transmitter reset signal.

5. The programmable logic resource of claim 2 wherein the circuitry further comprises a synchronizer associated with each of the plurality of channels, wherein:

each synchronizer is operative to take as input one of the plurality of reset signals and to

output the one of the plurality of reset signals at a beginning of a clock cycle.

6. The programmable logic resource of claim 5 wherein each synchronizer comprises a first flip-flop and a second flip-flop, wherein an output of the first flip-flop is sent as input to the second flip-flop.

7. The programmable logic resource of claim 5 wherein the circuitry further comprises logic circuitry that receives as input the output from each synchronizer and generates as output a single reset signal.

8. The programmable logic resource of claim 7 wherein the logic circuitry comprises an OR gate.

9. The programmable logic resource of claim 7 wherein the circuitry further comprises:

a second synchronizer in each of the plurality of channels operative to take as input the single reset signal and to output the single reset signal at a beginning of a clock cycle.

10. The programmable logic resource of claim 9 wherein the second synchronizer comprises a first flip-flop and a second flip-flop, wherein an output of the first flip-flop is sent as input to the second flip-flop.

11. The programmable logic resource of claim 1 further comprising control logic that receives as input the reset signal, a first signal, and a second

signal each generated from the programmable logic resource core circuitry, wherein the first signal and the second signal control when the reset signal is output from the control logic and sent as input to the circuitry.

12. The programmable logic resource of claim 11 wherein:

the first signal indicates when a supply voltage on the programmable logic resource core circuitry reaches a predetermined voltage level; and

the second signal indicates when programming of configuration data on the programmable logic resource core circuitry is completed.

13. A programmable logic resource having programmable logic resource core circuitry that provides a reset signal to an intellectual property block that supports a multi-channel input/output protocol comprising:

combinatorial logic that receives as input a reset signal and outputs a plurality of reset signals;

a central block coupled to the combinatorial logic having first circuitry operative to synchronize each of the plurality of reset signals and to output a single reset signal; and

second circuitry in each of a plurality of channels of the intellectual property block that is coupled to the central block and is operative to synchronize the single reset signal for output in each of the plurality of channels.

14. The programmable logic resource of claim 13 further comprising:

control logic that receives as input the reset signal, a first signal, and a second signal each generated from the programmable logic resource core circuitry, wherein the first signal and the second signal control when the reset signal is output from the control logic and sent as input to the combinatorial logic.

15. The programmable logic resource of claim 14 wherein:

the first signal indicates when a supply voltage on the programmable logic resource core circuitry reaches a predetermined voltage level; and

the second signal indicates when programming of configuration data on the programmable logic resource core circuitry is completed.

16. The programmable logic resource of claim 13 wherein each of the plurality of reset signals corresponds to one of the plurality of channels.

17. The programmable logic resource of claim 13 wherein each of the plurality of reset signals comprises a receiver reset signal.

18. The programmable logic resource of claim 13 wherein each of the plurality of reset signals comprises a transmitter reset signal.

19. The programmable logic resource of claim 13 wherein the central block having first circuitry comprises a synchronizer for each of the

plurality of reset signals, wherein each synchronizer outputs one of the plurality of reset signals at a beginning of a clock cycle.

20. The programmable logic resource of claim 19 wherein each synchronizer comprises a first flip-flop and a second flip-flop, wherein an output of the first flip-flop is sent as input to the second flip-flop.

21. The programmable logic resource of claim 19 wherein the central block having first circuitry further comprises:

a logic gate that receives as input the one of the plurality of reset signals from each synchronizer and outputs the single reset signal.

22. The programmable logic resource of claim 21 wherein the logic gate comprises OR circuitry that outputs a binary "1" when any one of its inputs is a binary "1."

23. The programmable logic resource of claim 13 wherein the second circuitry in each of the plurality of channels further comprises a synchronizer for the single reset signal, wherein the synchronizer outputs the single reset signal at a beginning of a clock cycle.

24. The programmable logic resource of claim 23 wherein the synchronizer comprises a first flip-flop and a second flip-flop, wherein an output of the first flip-flop is sent as input to the second flip-flop.

25. The programmable logic resource of claim 13 further comprising receiver circuitry coupled to the output of the second circuitry in each of the plurality of channels and operative to receive the single reset signal during a same clock cycle.

26. The programmable logic resource of claim 13 further comprising transmitter circuitry coupled to the output of the second circuitry in each of the plurality of channels and operative to receive the single reset signal during a same clock cycle.

27. A programmable logic resource comprising:

programmable logic resource core circuitry;

an intellectual property block that supports a multi-channel input/output protocol and is coupled to the programmable logic resource core circuitry, wherein the intellectual property block comprises reset circuitry that accepts as input a reset signal from the programmable logic resource core circuitry and outputs a synchronized reset signal that is distributed throughout each of a plurality of channels in the intellectual property block during a same clock cycle.

28. The programmable logic resource of claim 27 further comprising control logic operative to control input of the reset signal to the reset circuitry.

29. The programmable logic resource of claim 28 wherein the control logic is operative to

allow the reset signal to be sent to the reset circuitry when a supply voltage on the programmable logic resource core circuitry reaches a predetermined voltage level and when programming of configuration data on the programmable logic resource core circuitry is completed.

30. The programmable logic resource of claim 27 wherein the reset circuitry comprises combinatorial logic configured to generate a plurality of reset signals, wherein each of the plurality of reset signals corresponds to one of the plurality of channels in the intellectual property block.

31. The programmable logic resource of claim 30 wherein each of the plurality of reset signals comprises a receiver reset signal.

32. The programmable logic resource of claim 30 wherein each of the plurality of reset signals comprises a transmitter reset signal.

33. The programmable logic resource of claim 30 wherein the reset circuitry further comprises:

a first set of synchronizers that receives as input the plurality of reset signals and outputs each of the plurality of reset signals at a beginning of a clock cycle; and

a logic gate that receives as input the outputs from the first set of synchronizers and outputs a single reset signal that is routed to each channel.

34. The programmable logic resource of claim 33 wherein the reset circuitry further comprises:

a second set of synchronizers that

receives as input the single reset signal from the logic gate and outputs the single reset signal in each of the plurality of channels at a beginning of a clock cycle.

35. A digital processing system comprising:

processing circuitry;

a memory coupled to the processing circuitry; and

a programmable logic resource as defined in claim 27 coupled to the processing circuitry and the memory.

36. A printed circuit board on which is mounted a programmable logic resource as defined in claim 27.

37. The printed circuit board defined in claim 36 further comprising:

a memory mounted on the printed circuit board and coupled to the programmable logic resource.

38. The printed circuit board defined in claim 36 further comprising:

processing circuitry mounted on the printed circuit board and coupled to the programmable logic resource.